

Large area transistors get helping hand from quantum effects

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Researchers from the Hitachi Central Research Laboratory, Japan, and the Advanced Technology Institute of the University of Surrey today report that nano-designed transistors for the large area display and sensor application field benefit hugely from quantum size effects.

The unexpected superior switching performance (low leakage current, and steep sub-threshold slope) shown experimentally and analysed theoretically, demonstrate hitherto unexplored routes for improvements for transistors based on disordered silicon films.

By making the conduction channel in these disordered transistors very thin, the team has shown this technology will enable the design of low power memory for large area electronics based on a low-cost industry standard material processing route.

In the most recent investigations, the current of the devices, is found to be percolation governed when the channel is thinner than 3.0 nm due to strong quantum confinement induced potential variations over the active channel region. It is shown that the device channel width must be at least 0.3 μm to avoid percolative "pinch off" for 0.5 μm channel length devices. Theoretical analysis performed on the devices agrees well with the experimental data and provides important guidelines to model and optimize the devices for circuit design.

Dr Xiaojun Guo, one of the lead investigators, comments: "The nano-structure silicon thin-film transistors are very promising for design of

low power electronics. However, carrier transport in such devices is very complicated, and results in electrical characteristics that may not be described by conventional field effect transistor (FET) models. This work reveals the key physical properties of the devices, which will help to further optimize and model the devices for circuit design".

Professor Ravi Silva, Director of the Advanced Technology Institute adds: "This study is a prime example of how leading silicon technologies entrenched in industry can find alternative routes to improve on performance in device characteristics by clever design. The role that funding organizations such as EPSRC play in supporting this type of applied research is invaluable to the community and most importantly to industry".

The results are published in *Applied Physics Letters* 93 (2008) 042105.

Reference: X. Guo, S.R.P. Silva, T. Ishii, "Current percolation in ultrathin channel nanocrystalline silicon transistors", *Applied Physics Letters* 93, (2008) 042105.

Provided by University of Surrey

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