Integration Technologies for Complex Photonic Circuits

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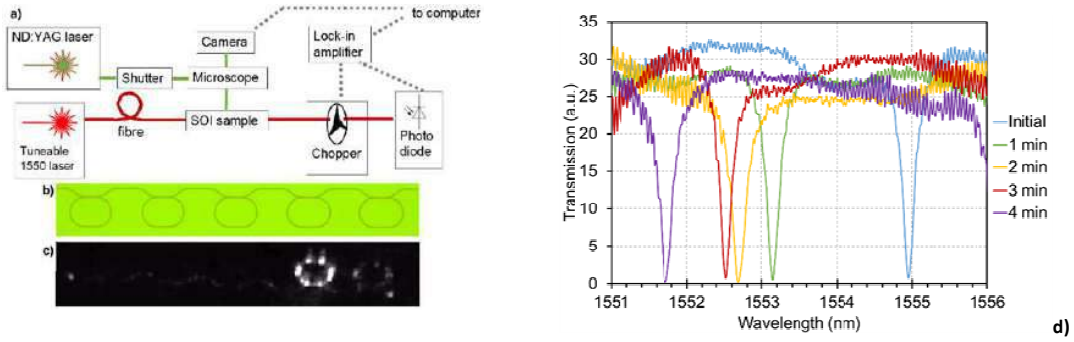
Abstract-Future photonic integrated chips for quantum experiments will demand several thousand of components and a number of diverse functionalities integrated on the same chip. We will discuss some of the challenges faced by the up-scaling of photonic integrated chips with a particular emphasis on robust component trimming and heterogeneous integration of III-V devices on a silicon-on-insulator platform.

The rapid increase in the complexity of quantum experiments demands a shift from bulk optics experiments to integrated circuits that can offer larger stability, compactness and low cost. Amongst the various material platforms, silicon-on-insulator (SOI) is of particular interest thanks to its large third-order nonlinearity, technological maturity and potential for large scale manufacturing. Moreover, its large index contrast allows for the design of very small bend radii that translates into high component density, with figures already exceeding thousands of components per chip[1,2].

However, component numbers and functionalities cannot indefinitely scale up if a number of issues are not effectively addressed. These include the development of algorithms, technologies and designs to mitigate the fabrication process variability, as well as manufacturing processes that allow wafer scale heterogeneous integration. The latter is of particular relevance to all those applications that require components such as optical sources, which cannot be provided by silicon. Here, we will focus on recent advances on trimming of silicon photonic components in complex circuits and on back-end integration of III-V membrane lasers by transfer printing.

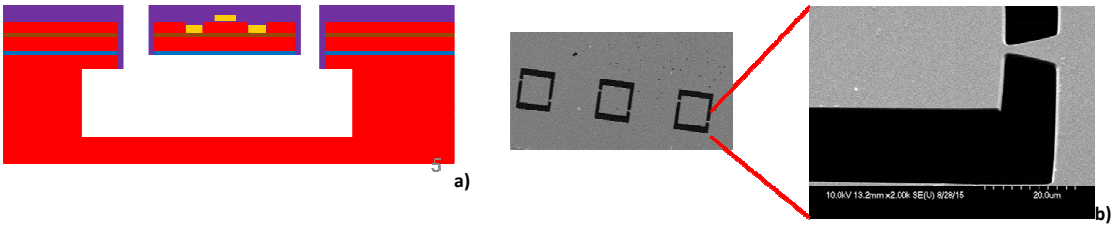
An effective way to trim optical components is to thermally cure a cladding layer on top of the silicon waveguide as a means to permanently change the effective index of the optical mode. We will discuss trimming techniques that offer long-term stability and wide tuning range through localised laser irradiation of the upper cladding (see Fig. 1).



Figures 1 a) Schematic of experimental set-up for localised trimming of SOI components using a frequency-doubled

ND:YAG laser. b) Micrograph of a racetrack resonator array and c) Racetrack array viewed in the infra-red while light is scattered from rings at resonance. d) Transmission spectra of a SOI racetrack resonator following thermal curing at 250℃ at 1 minute increments.

We will also present results on the transfer printing of III-V membrane devices onto silicon substrate with sub-micrometer positioning accuracy[3]. A notable advantage of this method, other than its scalability and precise alignment is the flexibility of the process. In fact, the bonding occurs after device fabrication, thus allowing independent fabrication processing of III-V and SOI wafers. Also, many different III-V membrane devices can be printed onto the SOI host substrate, with the potential for a wide range of heterogeneously integrated photonic devices. One such example is the integration of membrane materials with large Pockels coefficients for the development of ultra-fast electro-optic modulators.



Figures 2 a) Schematic showing the cross-section of a membrane device. b) SEM micrographs of III-V membranes with zooming in on the mechanical support tip

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