Matthew Chen

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Education

University of Waterloo Sep. 2024 – Apr. 2029
BASc in Electrical Engineering; ***GPA: 3.92/4.0*** *Waterloo, ON*
Scholarships: Intel, Presidential, and Non-Trivial
Relevant Coursework: Digital Circuits/Systems, Digital Computers, Electronic Circuits I/II, DSA

Work Experience

NVIDIA Feb. 2027 – Apr. 2027
Incoming ASIC Design Engineering Intern *Santa Clara, CA*
- Core CPU (interconnect and L3-cache) team

Altera May 2026 – Aug. 2026
Digital Systems Design Intern *Toronto, ON*
- Worked with AXI4 and AXI4-Lite protocols to facilitate transactions between FPGA fabric and HBM/CSR peripherals via External Memory Interfaces (EMIF), routing through the **Network on Chip (NOC)**
- Identified and addressed regtest holes in NOC configuration, generating new customer-facing cases with Quartus IP, leading to **30%** improved coverage of IP generation and synthesis
- Specced Test Engine IP block, optimizing within fabric constraints to log data stream on HBM for statistical debug

Marvell Sep. 2025 – Dec. 2025
Design Verification Intern *Ottawa, ON*
- Worked on **200G/lane optical retimer ASIC** for pluggable optical transceiver applications in datacenter interconnect
- Used Universal Verification Methodology **(UVM)** in SystemVerilog to verify transmitter-side (TX) functionality
- Developed new test plan for PRBS and fixed-pattern checkers by identifying coverage holes, adapted test for interleaved PAM4 checkers and verified by executing regressions and simulations, **improved coverage from 82% to 100%**
- Integrated Siemens Questa RDC/CDC into team flow for domain crossing/static analysis of (hard/soft) reset and clock trees
- Wrote testcases/assertions to improve functional/code coverage

Intel Jan. 2025 – Apr. 2025
RTL Design Intern *Toronto, ON*
- Authored Verilog digital design simulations, testbenches, and behavioural models for 112Gb/s SerDes
- Found non-critical post-tapeout RTL bug, constructed testbenches to verify and optimize asynchronous FIFO behaviour used for clock domain crossing (CDC), improved latency measurement accuracy by **70%**, impacted key design decision
- Performed RTL error assessment with Synopsys VC Lint and VC SpyGlass CDC
- Used SystemVerilog to model behaviour, generated and analyzed waveforms with Synopsys Verdi/VCS

Research and Projects

Director, Team Lead - Open-Source Ray-Tracing ASIC Jan. 2026 – Present
UWASIC Design Team *Waterloo, ON*
- Lead a team of 30 building an open-source ray-tracing ASIC on SkyWater 130 nm (SKY130); tapeout Q1 2027
- Supporting a variety of graphical primitives including matte/reflective surfaces, refraction, and emissive objects; proposed BVH encoding for 10x speedup during rendering
- Optimized and worked around extremely tight logic size constraints involving tapeout targeting the SKY130 node

FPGA Undergraduate Research Assistant Jan. 2026 – Apr. 2026
University of Waterloo *Waterloo, ON*
- Working with prof. Mina Arashloo and Kimiya Mohammadtaheri to build a protocol-agnostic transport-layer **FPGA accelerator** targeting AMD Alveo U250, co-author, submitted to ASPLOS 2027
- Implemented backpressure on data reassembly + packet generation modules, evaluated burst resilience for Ethernet TCP

Technical Skills

Hardware/HDL: Verilog/SystemVerilog, UVM, RISC-V, RTL Design, CDC/RDC, FPGA, VHDL
EDA Tools: Altera Quartus Prime, Synopsys (VCS/Verdi, SpyGlass), Siemens (Questa CDC/RDC), AMD Xilinx Vivado
Software: Python, IcarusVerilog/GTKWave, C/C++, Git(hub), Perforce, CUDA, PyTorch, NumPy, Matplotlib
Other: Linux/Unix, Altium/KiCad, STM32/Arduino, Confluence/Jira, LTSpice